Remarks

Applicant's novel processor comprises an architecture in which a plurality of multi-function processing layers are in data direct communication with a processing layer controller and perform data processing tasks in parallel to each other. It is fundamentally different from the prior art cited by Examiner.

In particular, it is fundamentally different than Lodenius. Lodenius teaches an architecture in which a plurality of functional units are in data communication with a selector (the Control and Radio Interface). The selector of Lodenius selects certain functional units to serially process data. Each of those functional units is in direct data communication with the selector and numerous other functional units. For example, the MCU BIU & Code Compaction unit (316) is in direct data communication with the Selector (302), SIM Interface (322), Display and Keyboard Drivers (324), DSP (306), MCU Serial Port (314), MCU (312), RF Control Interface (318), Power & Clock Management (320), and an External Bus (326).

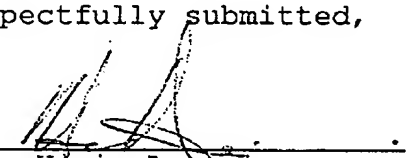
To that end, among numerous other differences, Lodenius does not teach "processing layers", as defined in the Applicant's specification. It teaches a plurality of functional units in data communication with other functional units. It also does not teach the parallel execution of tasks by processing layers and the restriction that the processing layers must be in direct data communication with only the selector and no other functional unit (i.e. an external bus). Rather, it teaches the serial assignment (selection) of certain functional units to process data and certain of those functional units are in direct data communication with functional units external to the chip, i.e. via an external bus.

Accordingly, Applicant has amended claim 1 to expressly include the fact that the system operates on a single chip,

thereby eliminating the applicability of Parameswaran Nair. Applicant has further incorporated into each independent claim the limitation: "wherein at least two of said processing layers receive tasks from said task scheduler and execute said tasks in parallel" and "wherein each of said processing layers is in direct data communication with said task scheduler and is not in direct data communication with any other functional unit". These additional limitations clearly differentiate the claimed inventions from the cited art.

Applicant believes that it has addressed Examiner's formal and informal rejections and submits that the current application is now in a form for allowance.

Respectfully submitted,

By 

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